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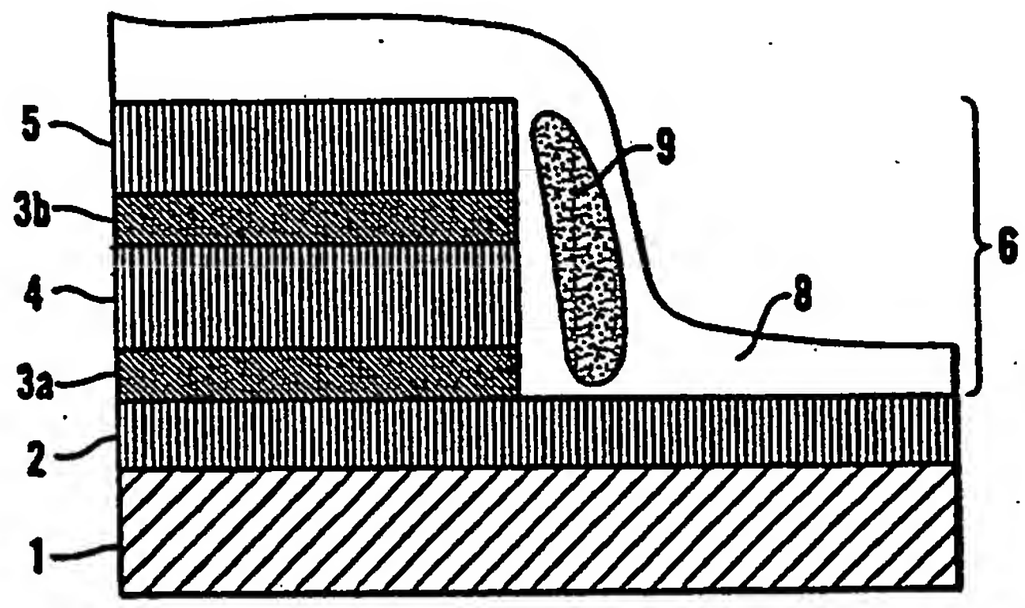


(57) Abstract

A field–effect transistor is made with electrodes (2, 4, 5) and isolators (3) in vertically provided layers, such that at least the electrodes (4, 5) and the isolators (3) form a step (6) oriented vertically relative to the first electrode (2) or the substrate (1). Implemented as a junction field–effect transistor (JFET) or a metal–oxide semiconducting field–effect transistor (MOSFET) the electrodes (2, 5) forming respectively the drain and source electrode of the field–effect transistor or vice versa and the electrode (4) the gate electrode of the field–effect transistor. Over the layers in the vertical step (6) an amorphous, polycrystalline or microcrystalline inorganic or organic semiconductor material is provided and forms the active semiconductor of the transistor contacting the gate electrode (8) directly or indirectly and forming a vertically oriented transistor channel (9) of the p or n type between the first (2) and the second (5) electrode. In a method for fabrication of a field effect transistor a vertical step (6) is formed by a means of a photolithographic process and a soluble amorphous active semiconductor material (8) is deposited over the first electrode (2) and the vertical step (6) such that a vertically oriented transistor channel between the drain and source electrode (2, 5) is obtained. In a JFET the semiconductor material (8) contacts the gate electrode (4) directly. In a MOSFET a vertically oriented gate isolator (7) is provided between the gate electrode (4) and the semiconductor material (8).

A field-effect transistor.

The present invention concerns field-effect transistors, respectively a junction field-effect transistor and a metal-oxide semiconductor field-effect transistor (MOSFET) with substantially vertical geometry, wherein the field-effect transistors comprise a planar substrate of non-conductive material. The invention also concerns a method for fabrication of field-effect transistors of this kind with a substantially vertical geometry, wherein the transistor comprises a planar substrate of non-conducting material.

Field-effect transistors (FET) which use an amorphous material as the active semiconductor are traditionally realized in a horizontal geometry such as rendered in fig. 1 which shows two examples (fig. 1a, fig. 1b) of the realization of a thin-film field-effect transistor according to prior art. Here the drain electrode and the source electrode are mutually separated by a transistor channel. This channel consists of an amorphous semiconductor material. The gate electrode is defined as a horizontal layer which is isolated from the channel by means of the gate isolator. The transistor effect is defined either as a depletion mode or an enrichment mode, depending on the gate potential. As the active amorphous semiconductor material in field-effect transistors of this kind conjugated polymers, aromatic molecules, and amorphous inorganic semiconductors have been used. For instance fig. 1 shows a thin-film transistor with an active semiconductor material in the form of amorphous Si:H in a 10 nm thick layer (D.B. Thomasson & al., IEEE El. Dev. Lett.,Vol. 18, p. 117; March 1997). A gate electrode which may be of metal, is provided on a substrate. An isolating layer of silicon nitride (SiN) is provided over this gate electrode and the active semiconductor material in form of amorphous Si:H is provided over the isolator in a 10 nm thick layer. The drain electrode and the source electrode are provided mutually spaced apart on the active semiconductor material. They are realized in a different metal than the gate electrode, for instance aluminium. Another example of an organic thin film transistor is shown in fig. 1b (A. Dodabalapur & al., Appl. Phys. Lett.; Vol. 69, pp.4227-29, December 1996). Here the active semiconductor material is an organic compound, for instance a polymer or aromatic molecules. As in the example in fig. 1a the gate electrode is provided on a substrate and above the gate electrode an isolator is provided in the form of a layer which may be made by coating the surface of the gate electrode with an oxide layer. something which may be

mutually spaced apart vertical side walls which at one end are connected with a similarly vertical end-wall. In the plane perpendicular to the walls the transistor channel hence obtains a U-shaped section, wherein the side walls are the legs of the U and the end wall the cross line. The walls may be provided on a suitable substrate and wholly covered by a layer of isolating material. A conducting layer which forms the gate electrode of the transistor is provided over the isolating layer. The ends of the side walls or the end of the U-shaped channel structure is exposed and on these end areas of the channel the source and drain electrodes respectively are formed, e.g. by means of an ion implantation process. The primary object of a thin film transistor of this kind is to provide a satisfying channel length on a smaller area than that which may be obtained with more conventional embodiments, while the leakage current is reduced when the transistor is in off-state.

The above-mentioned objects and other advantages are achieved according to the invention with a junction field-effect transistor (JFET) which is characterized in that a layer of conducting material which comprises a first electrode is provided on the substrate that a layer of isolating material which forms a first isolator is provided over the first electrode that a layer of conducting material which forms a second electrode is provided over the first isolator, that a further layer of isolating material which forms a second isolator is provided over the second electrode, that a layer of conducting material which forms a third electrode is provided over the second isolator, said first and third electrode respectively comprising the drain and source electrode of the transistor or vice versa and said second electrode the gate electrode of the transistor, that at least said second and said third electrode and said first and second isolator with the respective layers in stacked configuration form a step oriented vertically relative to said first electrode and/or said substrate, and that a semiconductor material which forms the active semiconductor of the transistor is provided over the exposed portion of said first electrode, said second electrode and said third electrode, said active semiconductor contacting the gate electrode directly and forming a substantially vertically oriented transistor channel between said first and said third electrode and a metal-oxide semiconductor field-effect transistor (MOSFET) which is characterized in that that a layer of conducting material which comprises a first electrode is provided on the substrate, that a layer of isolating material which forms a first isolator is provided over the first electrode, that a layer of conducting material which forms a second electrode

Where the field-effect transistor is a metal-oxide field-effect transistor (MOSFET) it is advantageous that an isolating material is being deposited on the vertical step in a vertically oriented layer, which is provided over the second electrode and forms the gate isolator in a field-effect transistor, the deposition taking place after the removal of said stacked configuration and said photoresist, but before the deposition of the soluble amorphous active semiconductor material.

It is according to the invention also advantageous that the active semiconductor material is an amorphous inorganic or organic semiconductor material, but need not be restricted to amorphous semiconductor materials, as it may also be selected among polycrystalline or microcrystalline inorganic or organic semiconductor materials.

Further features and advantages are apparent from the remaining appended dependent claims.

The invention shall now be discussed in greater detail with reference to the drawings wherein

fig. 1a	shows an example of prior art as mentioned above,
fig. 1b	another example of prior art as mentioned above,
fig. 1c	an example of a planar junction field-effect transistor according to prior art,
fig. 2	a preferred embodiment of a junction field-effect transistor according to the invention,
fig. 3	a preferred embodiment of a MOSFET according to the invention,
fig. 4a-e	the different process steps in an embodiment of the method according to the invention whereby the field-effect transistor is realized as a junction field-effect transistor, and
fig. 5a, 5b	further process steps in order to realize a MOSFET according to the invention.

Fig. 2 shows the embodiment of a junction field-effect transistor (JFET) according to the invention. It is wholly realized in thin-film technology, such as will be explained in more detail in the following. On a substrate 1 there is provided a layer 2 of a conducting material which forms a first electrode in the transistor. On this layer an isolating material 3a is provided which forms

the following. On a substrate 1 a layer 2 of conducting material is provided which forms a first electrode in the transistor. On this layer an isolating material 3a which forms a first isolator is provided and over the first isolator 3a a further conducting material is provided, for instance metal, which forms a second electrode in the transistor. On the second electrode 4 an isolating material 3b is provided which forms a second isolator in the transistor, and over the second isolator 3b a layer 5 of conducting material is provided which forms a third electrode of the transistor.

Realized as a MOSFET the first electrode 2 and the third electrode 5 now forms respectively the drain electrode and the source electrode of the transistor or vice versa. The second electrode 4 forms the gate electrode. Both the second and the third electrode 4;5 and isolators 3a, 3b are provided on the first electrode 2 such that they in relation to the first electrode 2 and the substrate 1 form a vertical step, the extension of which is indicated by the reference number 6 in fig. 2. Thus the structure consisting of the second and the third electrode 4,5 and the isolators 3 covers only a portion of the substrate 1 and the horizontal extension of the layers which form the vertical step 6 on the first electrode 2 or the substrate 1, may be made comparatively small.

Over the exposed vertical surface of the gate electrode 4 which is included in the vertical step 6, an isolating material 7 is provided which forms the gate isolator of the field-effect transistor. Over the top of the third electrode 5 which for instance may be the source electrode of the transistor, over the vertical step 6 and down to the first electrode 2 a layer of active semiconductor material is provided which may be an amorphous, polycrystalline or microcrystalline inorganic or organic semiconductor material. The gate electrode 4 is isolated against the active semiconductor material 8 by the gate isolator 7 such that charge injection is prevented. A substantially vertical transistor channel is defined in the active semiconductor material 8 and extends between the first electrode 2 and the third electrode 5 and substantially adjacent to the vertical step 6. Realized in this manner the structure shown in fig. 2 forms a metal-oxide semiconductor field-effect transistor (MOSFET). Optionally it may made with a first electrode 2 as drain electrode and the third electrode 5 as source electrode or vice versa. The transistor effect will either be given by a depletion mode or an enrichment mode, depending on the gate potential.

which forms the second electrode of the transistor, a second isolating layer 3b which forms the second isolator, and on the top thereof a layer 5 of conducting material which forms a third electrode of the transistor are provided sequentially. By using for instance a vapour deposition process the layers 3,4,5 now will cover both the exposed portion of the first electrode 2 and the top of the photoresist 10 in horizontally stacked layers, such as evident from fig. 4c.

In a fourth process step a lift-off method is now used for removing the layer on the top of the photoresist and the photoresist 10 itself. This is done by means of a solvent process, for instance with acetone. When the photoresist 10 and the layers on the top thereof are removed, the component appears as shown in fig. 4d after the fourth process step and with a step 6 vertically oriented relative to the first electrode 2 or the substrate 1.

Then a soluble amorphous active semiconductor material 8 is deposited over the first electrode 2, the second electrode 4 and the vertical step 6 and the top surface of the third electrode 5 in a fifth process step shown in fig. 4e. The active semiconductor 8 thus will cover the layer structures both horizontally and vertically. In case the first electrode 2 is patterned and only covers a portion of the substrate 1, for instance such that it itself forms a vertical step which is flush with the vertical step 6, there will in addition neither be a problem with the contact between the first electrode 2 and the active semiconductor material 8.

In the fabrication of a MOSFET in thin-film technology according to the invention an intermediate process step shown in fig. 5a is applied after the fourth process step shown in fig. 4d. In this further process step an isolating layer 6 is provided over the second electrode 4 such that the surface thereof is covered in the vertical step 6. This isolating layer 7 now comprises the gate isolator of the MOSFET and prevents charge injection. The gate isolator 7 may be made in a process where an oxide is provided with the first electrode 2 as substrate. Then a vertical etching step is used for forming the gate isolator 7 oriented in the vertical direction such that it covers the gate electrode 4. Alternatively the gate isolator 7 also could be provided by making the gate electrode 4 in a material which may be oxidized selectively or processed in one way or another such that an isolating layer is formed on

4e or fig. 5b, the individual transistors may be separated from the line and completed in the form of discrete components.

However, there is nothing against that greater portions of the line with a large number of transistors may form a transistor array which in its turn may be used for realizing active memory modules with the individual transistor as a memory element. The transistor must then be connected in a galvanic network by forming suitable conducting structures for the connections.

Generally vertical field-effect transistor as disclosed herein may be realized as structural parts in integrated electronic circuits in two and three dimensions. Possible applications of such circuits may be memories, processors etc. An obvious advantage of using active memory components based on transistors according to the present invention is the possibility of writing in small-signal mode and reading in large-signal mode, which particularly will be an advantage in electrical addressing of memory locations in large memory modules realized in a matrix network.

In regard of the fabrication process for the field-effect transistors according to the invention, it may as mentioned be realized globally by using continuous lines. In such a case it will also be possible to fabricate field-effect transistors as JFET and MOSFET with a vertical geometric structure by means of a printing method and not only by using well-known fabrication processes for VLSI components.

transistor or vice versa and said second electrode (4) the gate electrode of the transistor, that at least said second (4) and said third electrode (5) and said first (3a) and second isolator (3b) with the respective layers in stacked configuration form a step (6) oriented vertically relative to said first electrode (2) and/or said substrate (1), that a vertically oriented layer (7) of isolating material which forms a gate isolator is provided over said second electrode (4) and on said vertical step (6), and that a semiconductor material (8) which realizes the active semiconductor of the transistor and forms a substantial vertically oriented transistor channel (9) between said first (2) and said third electrode (5) is provided over the exposed portion of said first electrode (2), said vertical step (6) with said gate isolator (7) and said third electrode (5).

3. A field-effect transistor according to claim 1 or claim 2, characterized in that the first electrode (2) is provided patterned on the substrate (1) and forms a further intermediate step relative to the substrate (1), whereby every electrode (2, 4, 5) presents a substantially vertical surface to the active semiconductor (8).

4. A field-effect transistor according to claim 1 or claim 2, characterized in that the semiconducting material (8) is selected among amorphous, polycrystalline or microcrystalline inorganic or organic semiconductor materials.

5. A field-effect transistor according to claim 1 or claim 2, characterized in that the transistor channel (9) is defined as the vertical portion of the active semiconductor (8) between said first (2) and said third electrode (5) and adjacent to the vertical step (6) formed by the stacked configuration.

6. A field-effect transistor according to claim 1, characterized in that the semiconducting material (8) and the gate electrode (4) spontaneously form a Schottky junction (7).

7. A field-effect transistor according to claim 1, characterized in that the transistor channel (9) is defined as an n channel or p channel in the vertical portion of the active semiconductor (8) between said first (2) and second electrode (5) and adjacent to a pn junction at the gate electrode (4).

12. A method according to claim 11, characterized by the gate isolator (7) being formed as an oxide coating on the vertical surface of the gate electrode (4).

13. A method according to claim 12, characterized by the oxide coating (7) being formed by selective oxidation of the electrode material in the surface of the gate electrode (4).

14. A method according to claim 10, characterized by the first electrode (2) being deposited patterned on the substrate (1) and covering only partially the latter.

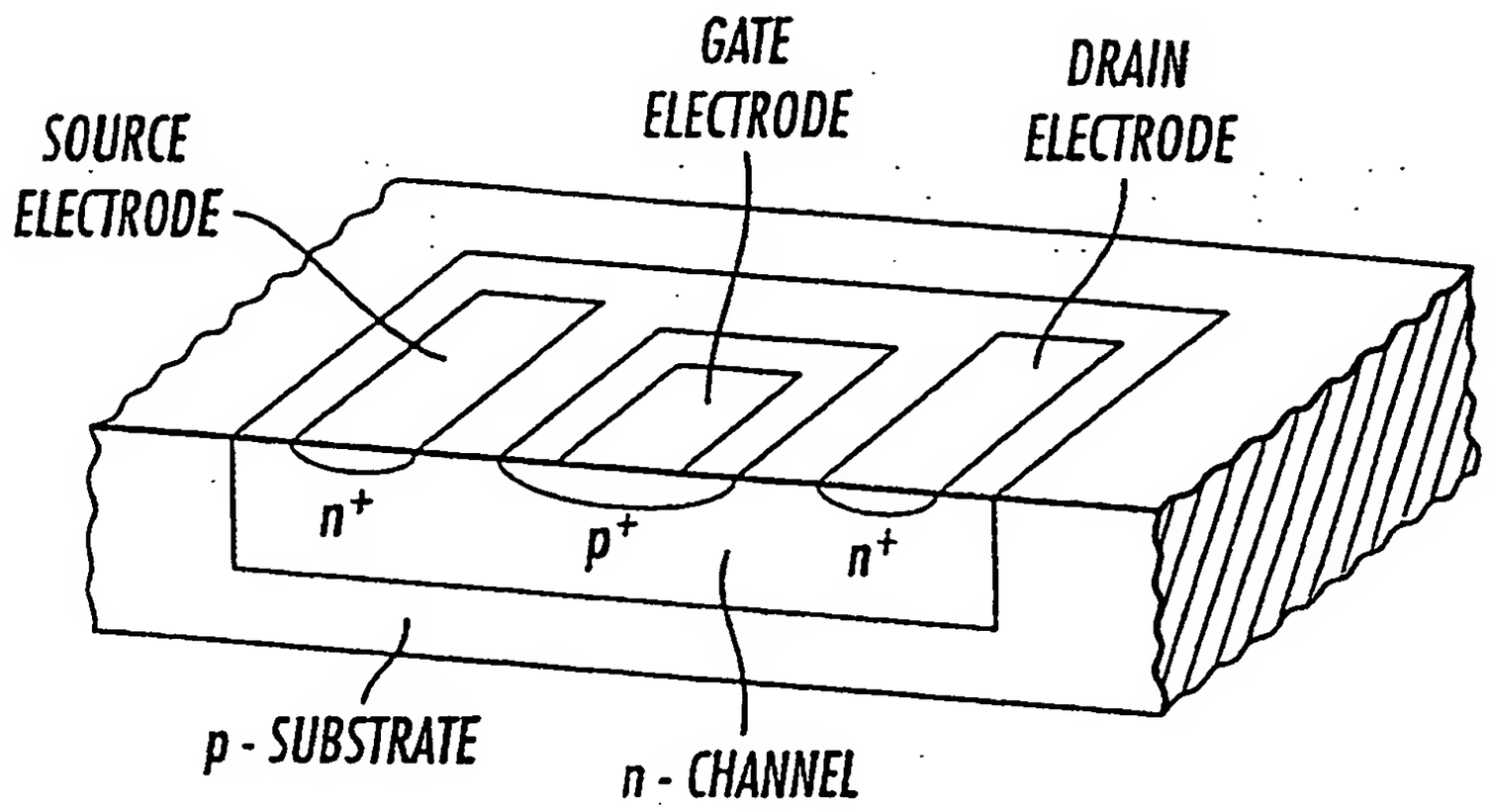

GATE ELECTRODE
DRAIN ELECTRODE
SOURCE ELECTRODE
n+
p+
n+
p - SUBSTRATE
n - CHANNEL

Fig.1c

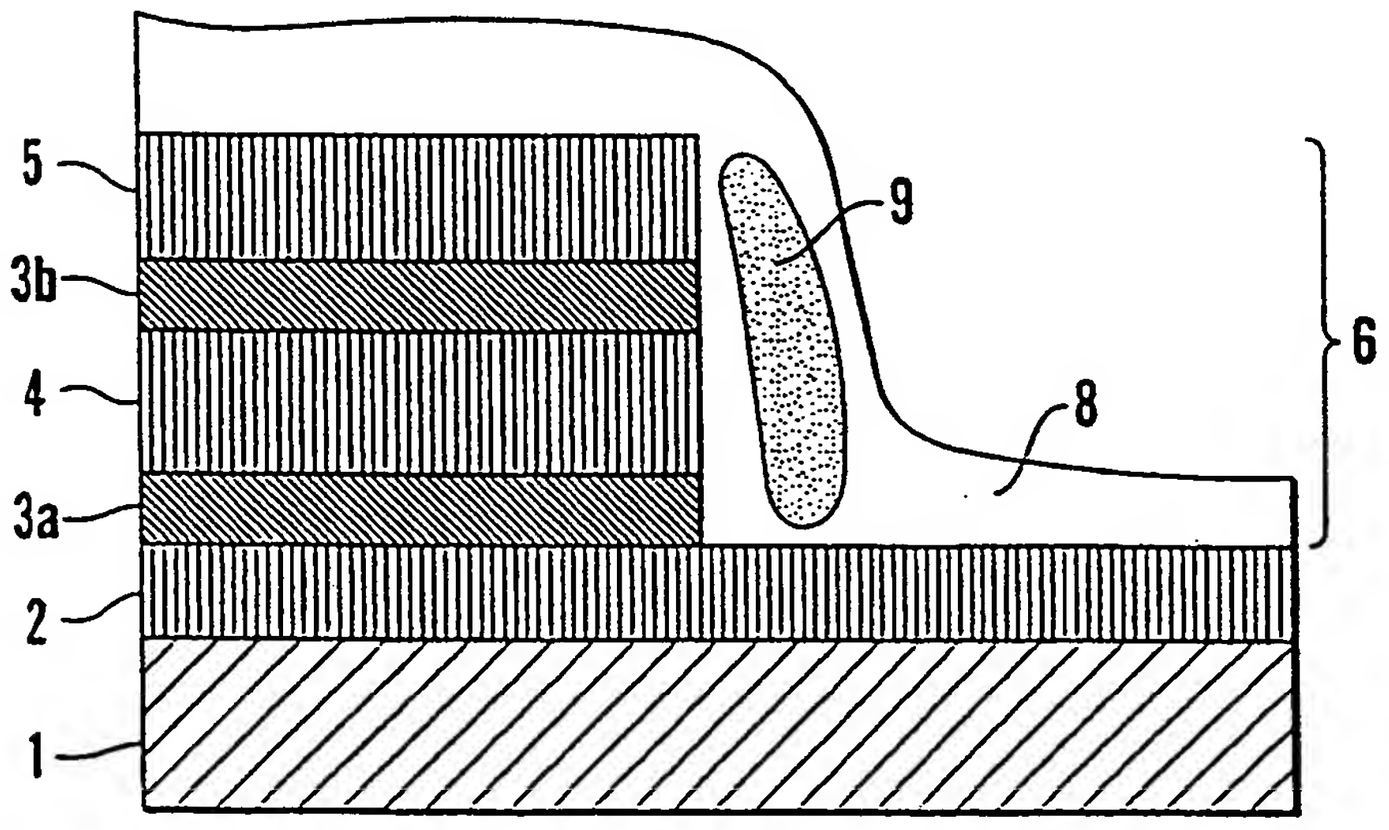
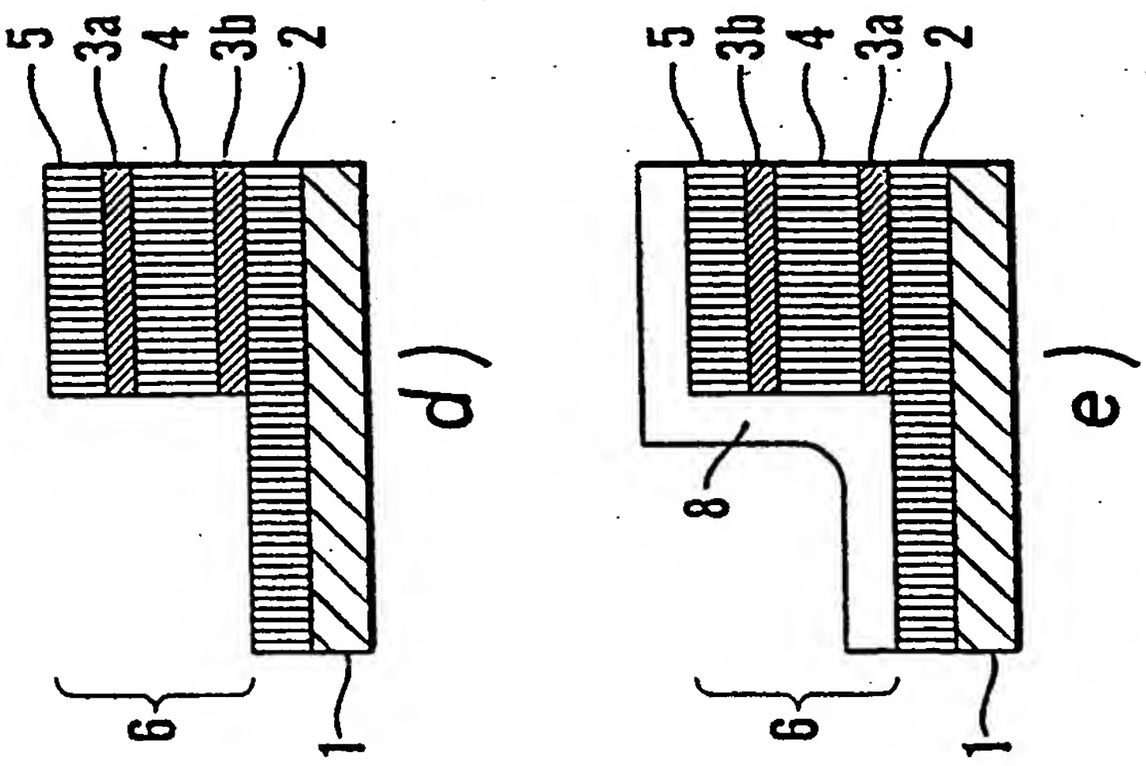

5
3b
4
3a
2
1
9
8
6

Fig.2



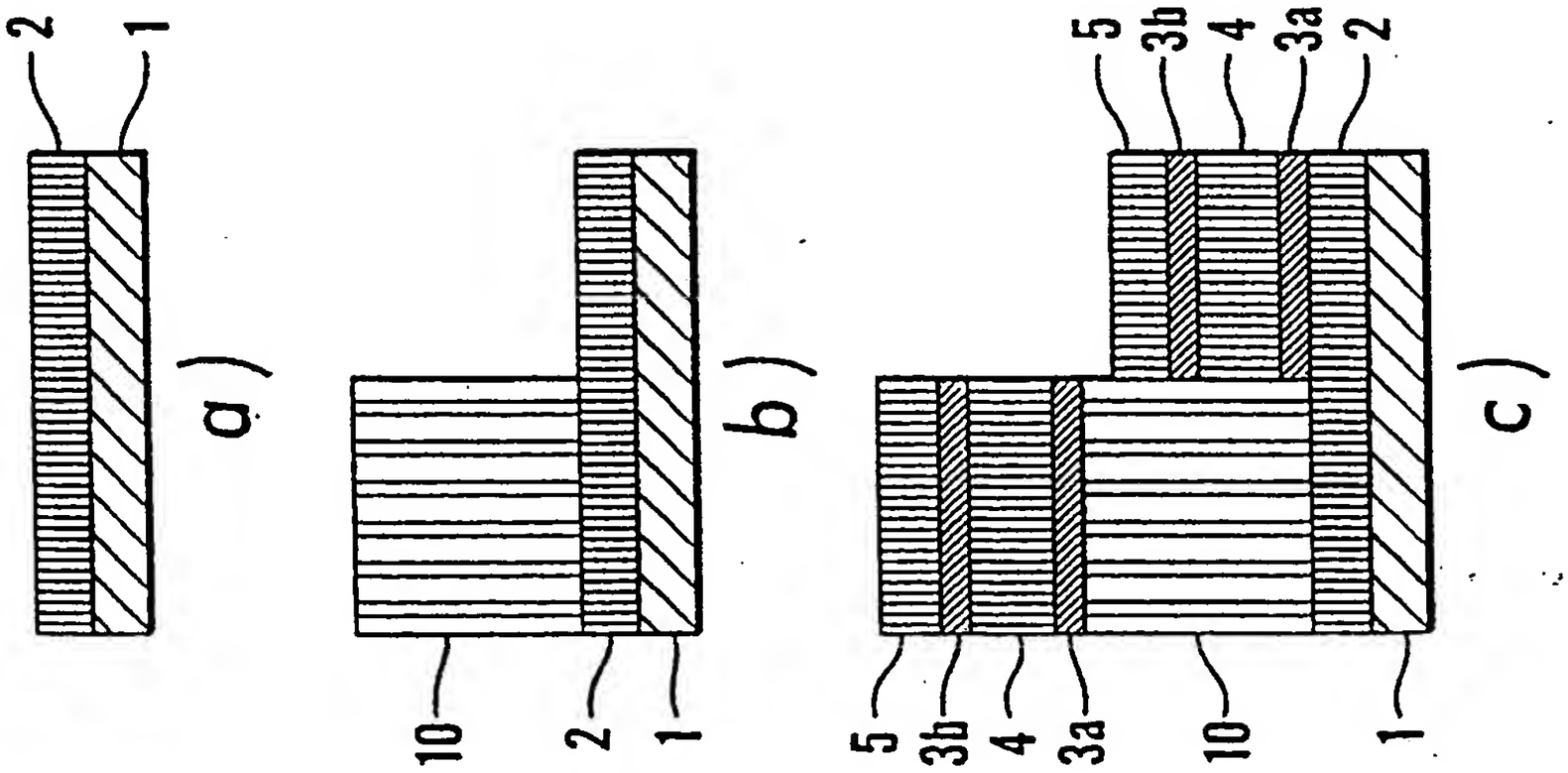


Fig.4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 99/00013

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 29/772, H01L 21/335, H01L 51/02
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EDOC, WPIL, JAPIO, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4677451 A (JAMES D. PARSONS ET AL), 30 June 1987 (30.06.87), column 3, line 57 - column 7, line 45	1,4,5,6
A	--	7-13
X	US 4735918 A (JAMES D. PARSONS ET AL), 5 April 1988 (05.04.88), column 3, line 58 - column 7, line 46	1,4,5,6
A	--	7-13
A	US 5047812 A (JAMES R. PFIESTER), 10 Sept 1991 (10.09.91), see whole document	2,4-13
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[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/NO 99/00013

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4677451 A	30/06/87	US 4735918 A	05/04/88
US 4735918 A	05/04/88	US 4677451 A	30/06/87
US 5047812 A	10/09/91	NONE	
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		JP 9232448 A	05/09/97
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		JP 1475123 C	18/01/89
		JP 58173870 A	12/10/83
		JP 63023669 B	17/05/88